

PAGE 4, PARAGRAPH 2 (a.k.a. lines 11-17) has been amended as follows:

The net result of feeding CK and CKD the clock input and the enable input, respectively,

of transparent latch **102** is a static to dynamic logic interface that is open until the inverse

5 of the dynamic logic evaluate clock rises falls. This static to dynamic logic interface also

remains closed until a delay element delay after the dynamic logic evaluate clock falls.

These properties help prevent hold time problems while providing timing benefits in an

easy to construct solution with low implementation cost.

10 IN THE CLAIMS:

CLAIMS 1-9 AND 13-16 have been canceled.

CLAIMS 10 AND 11 have been amended as follows:

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10. The interface of claim 9 wherein said latch comprises:A static logic to

dynamic logic interface, comprising:

a clock that is the inverse of a second clock that causes dynamic logic to evaluate;

a delay element that generates a delayed clock; and,

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a latch having a data input that interfaces to static logic, and an output that

interfaces to dynamic logic, and a first pass gate having a first pass gate

output, said first pass gate receiving said data input and being controlled

by said delayed clock; and,

clock, and a second pass gate having a second pass gate output that controls a

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latching node of said latch, said second pass gate receiving said first pass

gate output and being controlled by said clock.